Dynamic Testing of Xilinx Virtex-II Field Programmable Gate Array (FPGA) Input/Output Blocks (IOBs)

Gary M. Swift, *Member, IEEE*, Sana Rezgui, Jeffrey George, Carl Carmichael, Matthew Napier, John Maksymowicz, Jason Moore, Austin Lesea, R. Koga, and T. F. Wrobel

***Abstract*—Heavy-ion irradiation and fault injection experiments were conducted to evaluate the upset sensitivity of the Xilinx Virtex-II field programmable gate arrays (FPGAs) input/output block (IOB). Full triple module redundancy (TMR) of the IOBs, in combination with regular configuration scrubbing, proved to be a quite effective upset mitigation method.**

***Index Terms*—Fault injection, radiation effects, reconfigurable field programmable gate arrays (FPGAs), single-event effects.**

I. Introduction

SRAM-BASED field programmable gate arrays (S-FPGAs) are commonly used in telecommunication, wireless, networking, video and DSP applications on the ground and are increasingly considered for space environments. In contrast to antifuse based FPGAs, the interconnections that define a user design are determined by configuration data stored in an array of storage latches similar to a dual-port static random-access memory, allowing dynamic reconfiguration as often as desired. Xilinx S-FPGAs were used in the Mars Exploration Rover (MER) landers to control critical pyrotechnics during the landing sequence and they are also used to control the rover wheel motors. Although S-FPGAs are highly flexible, they are sensitive to single-event upsets (SEUs) from cosmic radiation. Recent work has focused on characterizing the SEU sensitivity of S-FPGAs with static and dynamic in-beam testing on the commercial Xilinx Virtex-II family [1]–[3].

S-FPGAs are complex, modern devices with many configurable choices that make comprehensive radiation testing difficult and expensive. A complementary method for studying the effect of SEUs is a simulation technique called fault injection (FI) in which errors are deliberately introduced into the FPGA configuration to see what effect they have on a targeted design.

In this paper we studied the SEU sensitivity of the input/output blocks (IOBs) used in the Xilinx Virtex-II 2V6000 FPGA using in-beam testing and fault injection with various mitigation methods to highlight the strengths and weaknesses of the two techniques. The IOBs are relatively complicated, configurable components associated with each of the several hundred general purpose pins on the Virtex-II device. In the course of this study we were also able to determine the relative effectiveness of two specific mitigation strategies which trade increased internal voting against greater use of limited input/output (I/O) resources.

II. FI Background

The literature suggests four basic types of FI techniques that were considered for application here: 1) software modification at the high level description of a given design [4]; 2) the total reloading of an SRAM-based re-configurable FPGA's contents [4], [5]; 3) the partial reconfiguration of a memory segment; and 4) the use of commercial software solution such as the Jbits tool [6], [7]. Upset simulation, a primary goal of this work, is not really possible with technique (i) and technique (iv) does not allow the level of control, visibility, and flexibility that a custom approach does. However, technique (ii) has been used successfully for upset simulation targeting an earlier Xilinx Virtex family device [8] and technique (iii), while previously untried, should be similarly successful and significantly faster. The selected target device, the Virtex-II 6000, is segmented into over 2000 configuration frames. Thus, the potential increase in speed (versus the full reconfiguration FI technique) is about a factor of 1000 (because the target frame must be accompanied by a second dummy frame to "activate" the target frame).

III. Experimental Setup

For dynamic radiation and FI experiments, a new board with an open socket for a Virtex-II 6000 device was designed by the Xilinx SEE Test Consortium[1] members and manufactured by the SEAKR Engineering. It includes two Xilinx FPGAs, their corresponding in-system programmable (ISP) configuration PROMs (XC18V04), and the required circuitry for the JTAG and SELECTMAP ports to access the FPGAs' configuration memory.

Manuscript received July 21, 2004. Some research presented here was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program (NEPP), Code AE and with the collaboration of Xilinx Inc. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer or otherwise does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

G. M. Swift is with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA (e-mail: gary.m.swift@jpl.nasa.gov).

S. Rezgui, C. Carmichael, J. Moore, and A. Lesea are with Xilinx, Inc., San Jose, CA 95124 USA (e-mail: sana.rezgui@xilinx.com).

J. George, J. Maksymowicz, and R. Koga are with the Aerospace Corporation, El Segundo, CA USA (e-mail: jeffrey.s.george@aero.org).

M. Napier and T. F. Wrobel are with Sandia National Laboratories, Albuquerque, NM USA (e-mail: mpnapie@sandia.gov).

Digital Object Identifier 10.1109/TNS.2004.839190

[1]The Xilix SEE Test Consortium, started by JPL and Xilinx, is a voluntary group of organizations the have a mutual interest in the evaluation of S-FPGAs for aerospace applications. The members combine resources and collaborate in order to obtain more sophisticated and efficient experimentation.

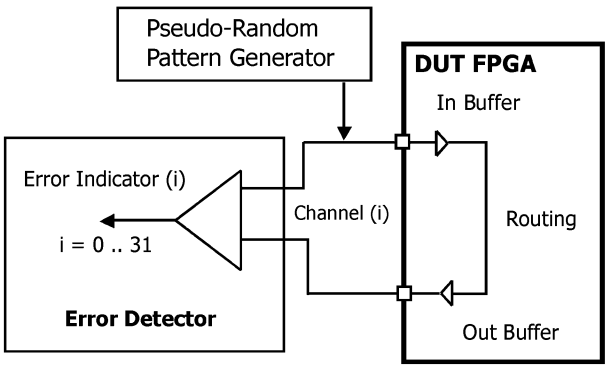

Fig. 1. Target Design 1 is the "No TMR" control case and has a single input connected with a minimum of routing to a single output and, thus, uses two external pins. Note "$i = 0.31$" indicates that the representative channel and error detector shown are duplicated 32 times, albeit with some differences in the length of the routing constructed by the design instantiation software.

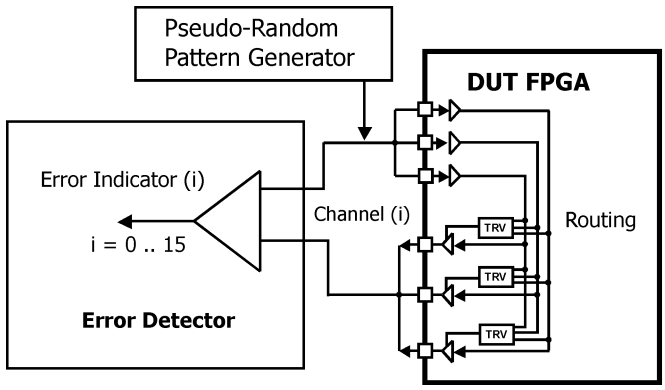

Fig. 2. Target Design 3 is the "Full TMR" case and uses three IOBs as triplicated inputs connected to three more IOBs as triplicated outputs using minimum routing and triplicated minority voters, labeled "TRV." Thus, each channel requires six pins.

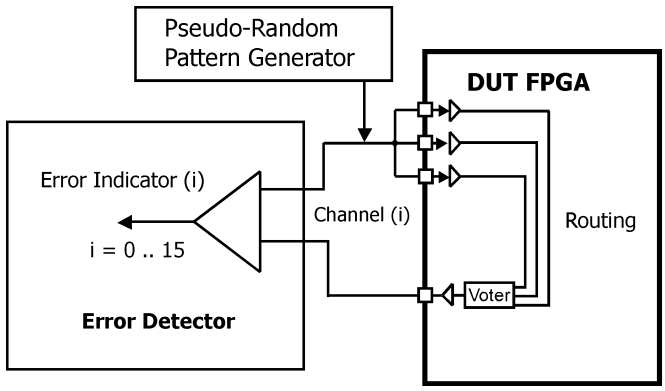

Fig. 3. Target Design 3 is the "TMR In-only" case and uses three IOBs as triplicated inputs connected to a single IOB for output using minimum routing and a single majority voter. Thus, each channel requires four pins.

The first FPGA is the Device Under Test (DUT), a radiation tolerant XQR2V6000, in an 1152-pin flip-chip fine-pitch package. It contains 144 18-Kbit block RAMs, 824 I/Os, and 16 395 508 configuration bits.

The second FPGA, an XQR2V3000-FG676, has two separate monitoring functions: 1) for configuration upsets and 2) for individual channel functionality. First, it serves as the configuration monitor (also called the "service FPGA") and is used for configuration, readback and scrubbing (the transparent process of reloading the configuration bitstream so upsets are corrected) of the DUT while it's being irradiated. The number of errors scrubbed is logged continuously on a host computer. Second, it serves as a functionality monitor for the target DUT design. In this role, the service FPGA sends a data stream to each DUT channel and continuously detects and counts the number of errors in the DUT IOBs by checking the outputs against the data sent. Any mismatches detected by the service FPGA are sent to a separate host computer via a custom visual basic software. More details about this testing methodology are given in [3]. For the testing reported here, the service FPGA feeds the channel inputs with a pseudorandom bitstream at 8 or 66 MHz and monitors the outputs for errors, counting them as they occurred.

IV. IOBs, TMR, and the Test Methodology

In the Virtex II architecture, IOBs connect to a pin and are configured as either an input or an output and programmed with electrical parameters required. They consist of an "input block," with an optional single or double data rate (SDR or DDR) register, an "output block," with an optional three-state SDR or DDR register plus an optional three-state high-current buffer, also with either a single or DDR register. There are several single-ended and differential I/O standard options available, including LVTTL, LVCMOS, PCI, GTL, and GTLP, HSTL, SSTL, and AGP-2X standards. Additionally, a digitally controlled impedance (DCI) feature provides configurable on-chip termination for each I/O element.

The target S-FPGA was configured with designs that implements multiple short "channels" of an input routed immediately to a nearby output. The simplest version of this is illustrated for one channel in Fig. 1; this was dubbed the "No TMR" design or Target Design #1. Using pins in close physical proximity minimizes the number of critical (or "used") configuration bits controlling routing resources; this maximizes the fraction of "used" bits that actually controls the IOBs' configuration.

It has been shown achieving maximum S-FPGA robustness to upset requires both TMR and configuration scrubbing [2]. To maintain operation of a design in the presence of a single configuration upset requires a TMR design, and frequent configuration scrubbings are needed to prevent the accumulation of errors. Detailed recommendations regarding TMR implementation for the Virtex family are given in an application note [12] and apply directly to the Virtex II also. "Full TMR" requires the use of three pins tied together externally both for the input and for the output, as illustrated in Fig. 2; this design was dubbed Target Design #2. Three minority voters add overhead and increase the number of configuration bits involved enough so that it is not clear whether the recommended scheme is superior to a simpler output scheme: a single majority voter to a single pin. This question is definitively answered in the experimental results below by comparing with the results of "Full TMR" and Target Design #3 which is shown in Fig. 3 and was dubbed the "TMR In-only" design.

V. Heavy Ion Upset Test Results

Table I lists beam details for the accelerated heavy ions used in the upset testing. Because the target device is only available

TABLE I
CHARACTERISTICS OF THE HEAVY ION BEAMS USED AT THE TEXAS A&M UNIVERSITY CYCLOTRON IRRADIATED THROUGH FLIP-CHIP DEVICES; SILICON THINNED TO 200 μm

Ion	Accelerated to MeV/amu	Energy (MeV)	LET	Range (microns)	Intervening media
Xe-129	24.8	977	56	86	In vacuum
Kr-78	40	2149	18.1	359	In air
Ar-40	24.8	623	7.5	242	In air

TABLE II
MEASURED IOB CROSS SECTIONS FOR LVCMOS I/O STANDARDS

Voltage	TMR Design	# of channels	LET	Fluence (ions/cm^2)	Broken Channels	Cross Section Per Channel (cm^2)	# of SEFIs
3.3 V	D1- No TMR	32	56	$0.43 \cdot 10^5$	7	5.1 *(+5.4, -3.1)* $\cdot 10^{-6}$	0
			18.1	$35.2 \cdot 10^5$	94	0.84 *(+0.17, -0.17)*$\cdot 10^{-6}$	3
3.3 V	D2- Full TMR	16	56	$2.7 \cdot 10^5$	0	0.0 *(+0.86, -0.0)* $\cdot 10^{-6}$	1
			18.1	$35.0 \cdot 10^5$	0	0.0 *(+0.066, -0.0)* $\cdot 10^{-6}$	6
			7.5	$67.3 \cdot 10^5$	0	0.0 *(+0.034, -0.0)* $\cdot 10^{-6}$	14
3.3 V	D3- TMR In only	25	56	$5.9 \cdot 10^5$	25	1.7 *(+0.8, -0.6)* $\cdot 10^{-6}$	3
		16	18.1	$40.7 \cdot 10^5$	46	0.71 *(+0.24, -0.19)*$\cdot 10^{-6}$	5
		16	7.5	$4.0 \cdot 10^5$	11	0.17 *(+0.14, -0.09)*$\cdot 10^{-6}$	2
1.8 V	D2- Full TMR	16	56	$46.0 \cdot 10^5$	1	0.15 *(+0.70, -0.14)*$\cdot 10^{-6}$	3
			7.5	$6.1 \cdot 10^5$	0	0.00 *(+0.38, -0.00)*$\cdot 10^{-6}$	0
1.8 V	D3- TMR In only	25	56	$3.1 \cdot 10^5$	9	1.2 *(+1.1, -0.7)* $\cdot 10^{-6}$	1
		16	7.5	$3.0 \cdot 10^6$	23	0.48 *(+0.24, -0.18)* $\cdot 10^{-6}$	3

in the flip-chip configuration, the beam reaches the active region only after penetrating the silicon substrate underlying the epitaxial layer. The substrate was thinned to 200 μm and the beam energies, ranges and LETs listed in Table I are the average parameters as the ions reach the active region. The applied internal bias on the configuration bits was 2.5 V in all cases and the testing was done at room temperature. The configuration scrub frequency (approximately 0.4 Hz) and the beam flux (between 23 and 350 ions/cm^2/s) were set so that less than 100 errors accumulated between scrubs for most of the irradiations.

Results for irradiation of these three designs configured for the LVCMOS I/O standard at two different standard voltages for the TMR versions are given in Tables II. Fig. 4 compares the LVCMOS 3.3 V results for the three target designs. As one would expect, the "No TMR" case is the worst of the three and the "Full TMR" is the best. Somewhat surprisingly, the "TMR In-only" design is only about a factor of two better than "No TMR."

In order to estimate the number of configuration bits involved in each measured cross section in Table II, the parameters for static upset cross section as a function of LET for configuration bits reported in [1] were used. These yield per bit cross sections of 5.5×10^{-8} cm^2 at LET $= 56$ and 2.4×10^{-8} cm^2 at LET $= 18.1$. Assuming that these values are applicable, the effective number of configuration bits in the unmitigated channel design (row 1 of Table II) is 91 bits at LET $= 56$ and 35 at

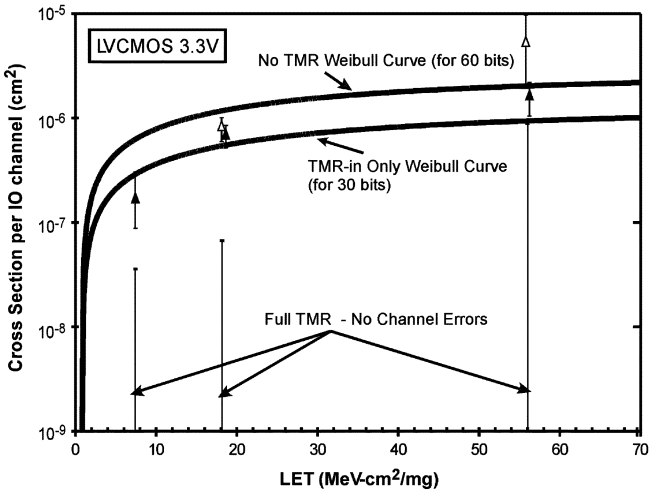

Fig. 4. Comparison of the heavy ion results for the three IOB designs for the case of LVCMOS 3.3 V. Note that the "Full TMR" design has yielded zero broken channels and, therefore, only the tops of the 95% error bars can be seen here.

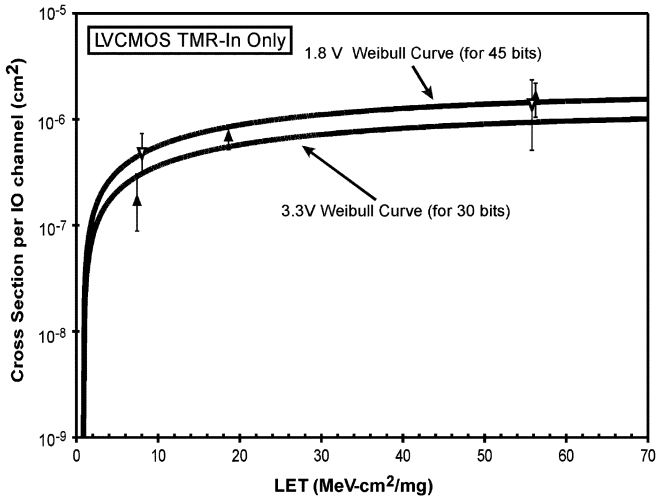

Fig. 5. Comparison of the heavy ion results for the "TMR In-only" IOB design for two voltages of LVCMOS. Differences, although expected, are not significant.

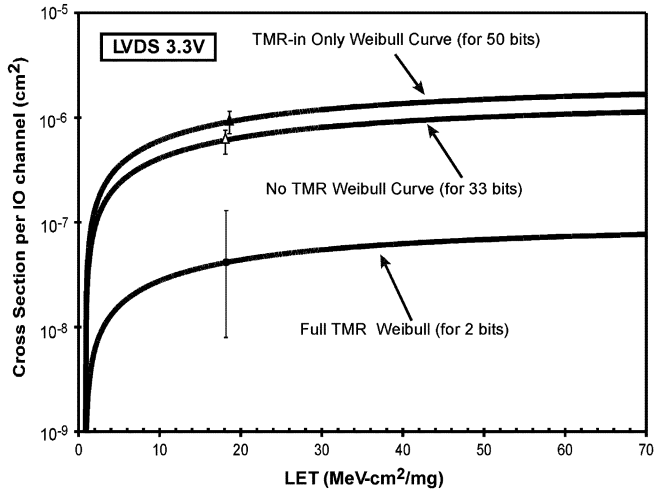

Fig. 6. Comparison of the heavy ion results for the three IOB designs for the case of LVDS 3.3 V.

$\mathrm{LET} = 18.1$; averaging these gives about 60 critical bits for the "No TMR" case. The Weibull curves for 60 and 30 bits are also shown in Fig. 4; the data suggests that the IOB configuration bits measured here, while clocking data through the XQR2V6000, have a somewhat different shape from that of the static cross sections previously measured for the XQ2V1000.

Fig. 5 compares the two voltages of LCMOS "TMR In-only" results as reported in Table II. Because the configurations should be almost identical, close results were expected. The lower voltage might have some increased cross section due to lowered margins and, therefore, increased vulnerability to single-event transients and/or output "fights" due to a hit crippling one of the minority voters. Fig. 5 shows the comparison is as expected: the 1.8 V results are similar to the 3.3 V results - or are showing a slight (perhaps 50%) increase in susceptibility.

See Fig. 6 and Table III for results on the three designs implemented with low-voltage differential signaling (LVDS) I/O standards. These runs were done with an order of magnitude higher flux of between 2100 and 4000 ions/cm^2/s. This higher flux should not affect the "No TMR" results, but would tend to increase measured susceptibility of the other designs because of the strong rate dependence of upset mitigation schemes, including TMR. Interestingly, these data suggest the "TMR-In Only" is worse than the "No TMR" case, although statistical significance is absent. They also show a significant advantage for "Full TMR," although a single observation of three channels breaking simultaneously did occur. This is likely due to the interaction of a group of two or more configuration upsets that individually would not cause a problem if present at separate times, exactly the type of coincidence engendered by the higher flux.

The last column of the tables gives the number of single-event functionality interrupts (SEFIs) observed. Observationally, SEFIs are defined here as an instance when all channels (7 to 32) stop working simultaneously. It should be noted that SEFIs are independent of design. Therefore, the cross section at a given LET can be derived from the sum of the values at that LET from the last column and the total fluence column of Table II, yielding, for example, at $\mathrm{LET} = 56$ MeV per mg/cm^2, eight SEFIs occurred during a total fluence of 5.8×10^6 cm^{-2} yielding a SEFI cross section of $1.4(+1.3, -0.8) \times 10^{-6}$ cm^2.

VI. FI Experiments

The purpose of FI is to identify sensitive bits in the configuration bits of a particular design. A sensitive bit is defined as a configuration bit that, when upset, disrupts the normal functional operation of the design. For the designs described in Section III, that means a broken channel.

To inject and repair faults, a new module, dubbed the FI Core, was developed to reside in the service FPGA along side and independent of the configuration and functional monitors. When the FI Core injects an error, the configuration monitor is used to confirm the presence of the simulated upset and the functional monitor determines whether one (or more) channels has been broken. Although the I/O stream is being clocked at 66 MHz and FI Core clocks the configuration port at 33 MHz, the functional monitor only reports errors about 30 times/s. Thus, it represents a significant bottleneck in the performance of the current FI setup.

In order to make the problem more tractable, a software tool developed by the Xilinx Research Laboratories called Single-Event Upset Probability Impact Tool (SEUPI) was used. This tool incorporates knowledge of the internal architecture controlled by the configuration bits and is able to identify all bits which are potentially sensitive in a particular design. The bits identified by the SEUPI tool are designated "used" configuration bits here. The SEUPI tool guarantees that the state of any single bit that it has not identified as "used" will not matter to the analyzed design. Further details of how SEUPI works can be found in [11].

SEUPI was used to identify all frames with "used" bits and the FI Core injected errors one-by-one in each of the 7872 bits in the identified frames. By observing the functional monitor, all sensitive bits can, thus, be identified.

Due to time constraints, FI experiments were performed only on the LVCMOS 3.3 V versions of the three target designs.

TABLE III
MEASURED IOB CROSS SECTIONS FOR LVDS I/O STANDARDS

Voltage	TMR Design	# of channels	LET	Fluence (ions/cm^2)	Broken Channels	Cross Section Per Channel (cm^2)	# of SEFIs
3.3 V	D1- No TMR	16	18.1	$1.00 \cdot 10^7$	96	0.60 *(+0.12, -0.12)* $\cdot 10^{-6}$	20
			7.5	$9.28 \cdot 10^4$	2	1.4 *(+3.5, -1.2)* $\cdot 10^{-6}$	0
3.3 V	D2- Full TMR	7	18.1	$1.01 \cdot 10^7$	1	0.042 *(+0.082, -0.034)* $\cdot 10^{-6}$	7
3.3 V	D3- TMR In only	8	18.1	$1.03 \cdot 10^7$	75	0.91 *(+0.21, -0.21)* $\cdot 10^{-6}$	20
2.5 V	D1- No TMR	16	7.5	$9.6 \cdot 10^6$	24	0.16 *(+0.08, -0.06)* $\cdot 10^{-6}$	5

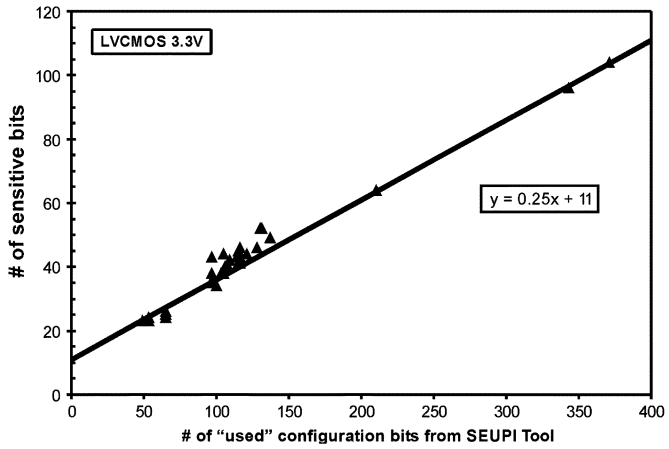

Fig. 7. Number of sensitive bits found by FI for each of the 32 channels of the "No TMR" design plotted as a function of the number of "used" bits for each channel reported by the SEUPI design analysis tool. The points should fall on the line shown if there are 11 (the intercept) sensitive bits in the IOB pair and if 25% of the routing bits are sensitive.

Comparisons of the SEUPI output for the LVCMOS 1.8 V designs showed that the voltage change added only a few bits, so the FI results would likely be the same. SEUPI had identified 20 to 46 frames with "used" bits. The FI experiments then were run, taking about 6 to 14 hours for every bit in the identified frames to be individually toggled.

In the case of the "No-TMR" design implemented with LVCMOS 3.3 V I/Os, the SEUPI tool has identified an average of 238 used bits per channel and has specified what they each configure: 55 bits control the input IOB, 63 bits the output IOB and an average of 120 bits are involved in the routing (varying from a minimum of 49 to a maximum of 371).

The following FI results were obtained for this case: only 11 bits controlling IOBs are sensitive. These 11 break down into 3 bits (out of 55 used bits) for the input IOB and 8 bits (out of 63 used bits) for the output IOB. Only an average of 32 bits controlling routing were discovered to be sensitive, ranging from 12 to 94 bits. The results of all 32 channels are shown in Fig. 7 where SEUPI-identified "used" bits (x-axis) are plotted against FI-identified sensitive bits. Even if SEUPI had not identified the type of configuration bit, a straight-line fit shows about eleven IOB bits (looking at the y-intercept).

The "Full-TMR" design implements 16 IOB channels. SEUPI identified that $165(3 \times 55)$ bits are used to define the triplicated input IOBs, $189(3 \times 63)$ bits for the triplicated output IOBs and an average of 568 bits (ranging from 482 to 640) are used for routing. FI results on the "Full-TMR" design prove that no single mis-configured bit can defeat the functional operation of a fully mitigated IOB channel.

The "TMR-In Only" design also implements 16 IOB channels. In this case, the SEUPI tool identified 228 used bits (165 allocated for the triplicated input IOBs and 63 bits for the single output IOB) in addition to an average of 202 routing bits (ranging from 178 to 230 bits). FI results show that no bits controlling input IOB are sensitive. On the output IOB side, the previously identified 8 bits sensitive in the "No-TMR" design, were again found to be classified as sensitive. This is as expected because only the input IOB was mitigated in this design. In addition, an average of 11 routing bits for each channel has been found to be disruptive of its functionality. This led to an average of 19 sensitive bits on every IOB channel, which is approximately the half of the counted sensitive bits for a "No-TMR" IOB channel (43 bits). This factor of two correlates well with the radiation results of the previous Section.

VII. DISCUSSION: COMPARING FI AND HEAVY ION RESULTS

This paper presents results for two complementary methodologies for SEU testing: in-beam upset results and FI experiments. The DUT is the XQR2V6000 from the Virtex-II S-FPGA family, and the example results focus on the I/O circuitry. The former (radiation testing) was tailored to directly measure the IOBs' upset cross-sections. The latter (FI) was used to identify the precise result of particular bit errors. That the two techniques give similar results can be seen in Table IV, although it appears that the beam results are about 50% higher. This discrepancy may be due to the effects of single-event transients in the data stream; the beam can cause transients and FI cannot. Also, either the occurrence of coincident errors from multiple ion strikes within a scrub window or multiple upsets from a single ion strike may explain the difference. These hypotheses will be sorted out using a new capability being developed that uses a communication channel between the configuration monitor and the functional monitor. When an interesting event, such

TABLE IV
COMPARISON OF THE COUNTS OF SENSITIVE BITS FROM FAULT INJECTION AND BEAM UPSETS

3.3V LVCMOS Design	FI	Beam
No TMR	43	60
Full TMR	0	0
TMR-In Only	19	30

as a channel's functionality is broken, the functional monitor will signal the configuration monitor to forego scrubbing momentarily and capture the current configuration for later analysis. If SEUPI and/or FI can confirm that none of the upset bits in the configuration alone can account for the broken channel, then FI will be used to determine if any pairs of bits are responsible. If not, then by elimination, the transient explanation is the correct one. It is interesting to note that the new in-beam capture capability is really only useful in conjunction with FI.

VIII. CONCLUSION

Two specific conclusions can be drawn here. First, the recommended TMR using three input pins and three output pins is very effective at mitigating functional problems caused by a configuration upset (in conjunction with configuration scrubbing). Second, "partial" TMR on I/Os, such as the "TMR In-only case," adds only a small increment of upset mitigation.

General conclusions may be reached inductively from the IOB beam and FI investigations. First, the FI technique appears most useful as an adjunct to upset testing where additional or more precise information needs to be developed. Thus, the two techniques are complementary. While FI can reduce the beam time needed for upset characterization, the results of FI need some irradiation data for calibration and also to validate that upsets that cannot be simulated by faults do not dominate in-beam results. Second, the use of partial reconfiguration allows faults to be injected relatively quickly; this results in the speed of the functional testing limiting the speed of FI. Finally, FI cannot fully replace heavy ion irradiation, not only because threshold LET must be found with the beam, but also because the beam can induce transients and FI cannot; transients do appear to be important at the speeds of modern devices.

REFERENCES

[1] C. Yui, G. Swift, and C. Carmichael, "Single event upset susceptibility testing of the xilinx virtex II FPGA," in *Int. Conf. Military and Aerospace Applications of Programmable Logic Dev.*, Sept. 2002.

[2] C. Yui, G. Swift, C. Carmichael, R. Koga, and J. George, "SEU mitigation testing of Xilinx Virtex II FPGAs," in *Radiation Effects Data Workshop Record*, 2003, pp. 92–97.

[3] R. Koga, J. George, G. Swift, C. Yui, C. Carmichael, T. Langley, P. Murray, K. Lanes, and M. Napier, "Comparison of Xilinx Virtex-II FPGAs SEE sensitivities to protons and heavy ions," in *Proc. 7th Eur. Conf. Radiation and Its Effects on Components and Systems*, Sept. 2003.

[4] T. Delong, B. Johnson, and J. Profeta, "A fault injection technique for VHDL behavioral-level models," *IEEE Des. Test Comput.*, vol. 13, pp. 24–33, Winter 1996.

[5] F. Lima, C. Carmichael, J. Fabula, R. Padovani, and R. Reis, "A fault injection analysis of Virtex FPGA TMR design methodology," in *Proc. 6th Eur. Conf. Radiation and Its Effects on Components and Systems*, Sept. 2001, pp. 275–282.

[6] L. Antoni, R. Leveugle, and B. Feher, "Using run-time reconfiguration for fault injection applications," *IEEE Trans. Instrum. Meas.*, vol. 52, no. 5, Oct. 2003.

[7] M. Caffrey, P. Graham, E. Johnson, and M. Wirthlin, "Single-event upsets in SRAM FPGAs," in *Int. Conf. Military and Aerospace Applications of Programmable Logic Devices*, Sept. 2002.

[8] M. Alderighi, F. Casini, S. D'angelo, M. Mancini, A. Marmo, S. Pastore, and G. Sechi, "A tool for injecting SEU-like faults into the configuration control mechanism of Xilinx Virtex FPGAs," in *Proc. 18th IEEE Int. Symp. Defect and Fault Tolerance in VLSI Systems*, Nov. 2003.

[9] G. Swift, C. Yui, and C. Carmichael, "Mitigating upsets in SRAM-based FPGAs from the xilinx virtex 2 family," in *Int. Conf. Military and Aerospace Applications of Programmable Logic Devices*, Sept. 2003.

[10] P. Graham, M. Caffrey, M. Wirthlin, E. Johnson, and N. Rollins, "SEU mitigation for half-latches in xilinx virtex FPGAs," *IEEE Trans. Nucl. Sci.*, vol. 50, pp. 2139–2146, Dec. 2003.

[11] P. Sundararajan, C. Patterson, C. Carmichael, S. McMillan, and B. Blodget, "Estimation of single event upset probability impact of FPGA designs," in *Int. Conf. Military and Aerospace Applications of Programmable Logic Devices*, Sept. 2003.

[12] C. Carmichael. (2001, Nov.) Triple module redundancy design techniques for Virtex FPGAs. *Xilinx Application Note XAPP197* [Online]. Available: www.xilinx.com/bvdocs/appnotes/xapp197.pdf